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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/656,984	09/07/2000	Anthony M. Chiu	00-C-016	2247

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EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action

Application No.	Applicant(s)	
09/656,984	CHIU, ANTHONY M.	
Examiner	**Art Unit**	
Khiem D Nguyen	2823	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 14 October 2002 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *see office action*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *1-8,21-25 and 29-31*.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☒ Other: *see office action*

DETAILED ACTION

Response to Amendment after final or Advisory Action

1. Applicant's arguments filed 10-14-2002 have been fully considered but they are not persuasive.

Status of the amendment after final rejection

D. Others: the amendments in claim [1] would be entered for purposes of appeal if submitted separately.

Status of the pending claims after final rejection

1. The finally rejected claims are 1-8, 21-25, and 29-31.

Status of the Pending Rejections or Objections

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crane, Jr. et al. (USPN. 6,307,258 B1) hereinafter Crane in view of Ichikawa et al. (USPN. 6,165,818) herein after Ichikawa.

With respect to claim 1, Crane show a method of providing electrostatic discharge protection (Figs. 1-2 #100 col. 3 line 62) for an integrated circuit (Figs. 1-2 #10 col. 3 line 57), comprising:

mounting an integrated circuit die (Figs 1-2 # 10 col. 3 line 62) on a lead frame (Figs. 1-2 # 200 col. 3 line 62); encapsulating (col. 4 line 36-40) at least part of the

integrated circuit die with a plastic or epoxy material (See col. 4 lines 5-8); and show folding an unencapsulated portion of the lead frame around sides of the encapsulated integrated circuit die (# 100) but fails to show folding an un-encapsulated portion of lead frame over or adjacent to a peripheral upper surface of the plastic or epoxy material as required in the present claim. However, ***it would have been obvious to one of ordinary skill in the art*** to show folding an un-encapsulated portion of the lead frame over or adjacent to a peripheral upper surface of the plastic or epoxy material as required in the present claim, because selection of any order of performing process steps is prima facie obvious in the absence of new of unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

With respect to claim 2, Crane shows the steps of connecting the portion of the lead frame (Figs. 1 and 2. # 200 col. 3 line 61) around sides of the encapsulated integrated circuit die (Fig. 1 # 100 Col. 3 line 62) and over or adjacent to a peripheral upper surface of the plastic or epoxy material (See col. 4 lines 5-8) but fails to show connection to a ground voltage.

Ichikawa shows a pair of radiating terminals (Figs 1-2 # 2 col. 1 line 64) of the lead frame (Figs. 1-2 # 12 col. 2 line 8) are connected to grounding lines of the circuit board (See col. 1 lines 59-65).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to show the method of Ichikawa in the process of Crane for connecting some terminals of the lead frame to a ground voltage because in doing so

various signals can be inputted to and outputted from the pallet and extra heat is radiated from ground terminals. (See Ichikawa col. 1 lines 66-67 and col. 2 lines 1-2).

With respect to claim 3, Crane show the steps of encapsulating at least part of the integrated circuit die (# 100) with a plastic or epoxy material further comprising: After mounting the integrated circuit die (# 100) on the lead frame (# 200), encapsulating exposed surfaces of the integrated circuit die except for a sensing surface (See Crane col. 4 lines 25-27); and encapsulating wire bonds (Crane Col. 4 lines 12) connecting the integrated circuit die (# 100) through leads (# 300) to portions of the lead frame (# 200). (See crane Figs. 1-2 col. 4 lines 11-18 and col. 4 lines 25-30).

With respect to claim 4, Crane in view of Ichikawa show the steps of folding a portion (Ichikawa outer portions Fig. 3 # 5 and # 6 of terminals # 2 and # 3 col. 1 line 56) of the lead frame (Ichikawa Fig. 3 # 11 col. 2 line 7) around sides of the encapsulated integrated circuit die (Ichikawa Fig. 1 # 4 col. 1 line 52) and over or adjacent to a peripheral upper surface of the plastic or epoxy material (# 4). (See Ichikawa col. 1 lines 50-58), folding portions (Ichikawa Fig. 4 # 32, # 33 col. 6 line 58) of the lead frame (Ichikawa Fig. 4 # 41 col. 6 line 47) around each side (Fig. 4 col. 6 lines 52-54) of the encapsulated integrated circuit die (Ichikawa Fig. 4 # 31 col. 6 line 48). (See Ichikawa Figs.1-2 and Figs. 3-7).

With respect to claim 5, Crane in view of Ichikawa show the steps of folding a portion (Ichikawa outer portions Fig. 3 # 5 and # 6 of terminals # 2 and # 3 col. 1 line 56) of the lead frame (Ichikawa Fig. 3 # 11 col. 2 line 7) around sides of the encapsulated integrated circuit die (Ichikawa Fig. 1 # 4 col. 1 line 52) and over or adjacent to a

peripheral upper surface of the plastic or epoxy material (# 4), and Ichikawa further teach the steps of folding portions (Ichikawa, Fig. 4 # 32, # 33 col. 6 line 58) of the lead frame (Ichikawa Fig. 4 # 41 col. 6 line 47) around each side (Fig. 4 col. 6 lines 52-54) of the encapsulated integrated circuit die (Ichikawa Fig. 4 # 31 col. 6 line 48). (See Ichikawa Figs. 1-2 and Figs. 3-7).

folding a first portion (Ichikawa Figs. 4-6 # 47 of terminal # 33 and 48 of terminal # 32 col. 6 lines 52-65) of the lead frame (Figs. 5 and 6 # 41) around a first side of the encapsulated integrated circuit die (Figs. 5 and 6 # 31 col. 7 line 40), wherein the first portion includes an opening (# 37 col. 7 line 43) providing access for a connector (# 44 col. 7 line 47) to pins (Fig. 5 # 45 col. 7 line 48) electrically connected to the integrated circuit die (Figs. 5 and 6 # 31 col. 7 lines 21-26).

folding a first portion (Ichikawa Figs 5 and 6 # 35 and # 36 col. 7 line 41 of terminal # 32 and # 33 col. 7 lines 42-43) of the lead frame (Figs. 5 and 6 # 41) around a first side of the encapsulated integrated circuit die (Figs. 5 and 6 # 31 col. 7 line 40), wherein the first portion includes an opening (# 37 col. 7 line 43) providing access for a connector (# 44 col. 7 line 47) to pins (Fig. 5 # 45 col. 7 line 48) electrically connected to the integrated circuit die (Figs. 5 and 6 # 31 col. 7 line 39).

With respect to claim 6, Crane in view of Ichikawa show the steps of folding a portion (Ichikawa outer portions Fig. 3 # 5 and # 6 of terminals # 2 and # 3 col. 1 line 56) of the lead frame (Ichikawa Fig. 3 # 11 col. 2 line 7) around sides of the encapsulated integrated circuit die (Ichikawa Fig. 1 # 4 col. 1 line 52) and over or adjacent to a peripheral upper surface of the plastic or epoxy material (#4), and Ichikawa further teach

the steps of folding portions (Ichikawa Fig. 4 # 32, # 33 col. 6 line 58) of the lead frame (Ichikawa Fig. 4 # 41 col. 6 line 47) around each side (Fig. 4 col. 6 lines 52-54 of Ichikawa Figs. 1-2 and Figs. 3-7).

folding a portion (Ichikawa Figs 4-6 terminals # 35 and # 36 col. 7 lines 40-45) of the lead frame (Figs. 5 and 6 # 41) around edges of the encapsulated integrated circuit die (Figs. 5 and 6 # 31 col. 7 line 40), not including leads (# 32 and # 33) electrically connected to the integrated circuit die (# 31).

With respect to claim 7, Crane in view of Ichikawa show the steps of folding a portion (Ichikawa outer portions Fig. 3 # 5 and # 6 of terminals # 2 and # 3 col. 1 line 56) of the lead frame (Ichikawa Fig. 3 # 11 col. 2 line 7) around sides of the encapsulated integrated circuit die (Ichikawa Fig. 1 # 4 col. 1 line 52) and over or adjacent to peripheral upper surface of the plastic or epoxy material (# 4), and Ichikawa further teach the steps of folding portions (Ichikawa Fig. 4 # 32, # 33 col. 6 line 58) of the lead frame (Ichikawa Fig. 4 # 41 col. 6 line 47) around each side (Fig. 4 col. 6 lines 52-54) of the encapsulated integrated circuit die (Ichikawa Fig. 4 # 31 col. 6 line 48). (See Ichikawa Figs. 1-2 and Figs. 3-7).

folding a first portion (Ichikawa Figs. 4-6 # 47 of terminals # 33 and 48 of terminals # 32 col. 6 lines 52-65) of the lead frame (Figs. 5 and 6 # 41) around a side of the encapsulated integrated circuit die (Figs. 5 and 6 # 31 col. 7 line 40); and folding a second portion (# 35 and # 36 of terminal # 32) of the lead frame (# 41) extending from the first portion over a peripheral upper surface of the encapsulated integrated circuit die (# 31). (See col. 7 lines 41-45).

With respect to claim 8, Crane in view of Ichikawa show the steps of folding a portion (Ichikawa outer portions Fig. 3 # 5 and # 6 of terminals # 2 and # 3 col. 1 line 56) of the lead frame (Ichikawa Fig. 3 # 11 col. 2 line 7) around sides of the encapsulated integrated circuit die (Ichikawa Fig. 1 # 4 Col. 1 line 52) and over or adjacent to a peripheral upper surface of the plastic or epoxy material (# 4), and Ichikawa further teach the steps of folding portions (Ichikawa Fig. 4 # 32, # 33 col. 6 line 58) of the lead frame (Ichikawa Fig. 4 # 41 col. 6 line 47) around each side (Fig. 4 col. 6 lines 52-54) of the encapsulated integrated circuit die (Ichikawa Fig. 4 # 31 col. 6 line 48). (See Ichikawa Figs. 1-2 and Figs. 3-7).

folding a first portion (Ichikawa Figs. 4-6 # 47 of terminal # 33 and 48 of terminal # 32 col. 6 lines 52-64) of the lead frame (Figs. 5 and 6 # 41) around a side of the encapsulated integrated circuit die (Figs. 5 and 6 # 31 col. 7 line 40); and folding a second portion (# 35 and # 36 of terminal # 32) of the lead frame (# 41) extending from the first portion adjacent to and level with a peripheral upper surface of the encapsulated integrated circuit die (# 31). (See col. 6 lines 66-67 and col. 7 lines 1-4).

3. Claims 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crane, Jr. et al. (U.S. Patent 6,307,258) in view of Ichikawa et al. (U.S. Patent 6,165,818).

Crane teaches a method of providing electrostatic discharge protection for an integrated circuit, comprising (See Col. 3, line 56 to col. 5, line 30 and FIGS. 1).

mounting the integrated circuit die 100 on a flat lead frame 200, 300 having the lead portions projecting at least one edge and the electrostatic discharge protection portion projecting from at least one edge wherein the electrostatic discharge protection

portion of the lead frame projects from an edge other than an edge from which the lead portions project;

encapsulating at least part of an integrated circuit die 100 mounted on a lead frame 200, 300 and a portion of the lead frame with a plastic or epoxy material, leaving lead portions and an electrostatic discharge protection portion of the lead frame un-encapsulated and further comprising forming the plastic or epoxy material over one surface and sidewalls of the integrated circuit die and over portions of a surface of the lead frame on which the integrated circuit die is mounted, leaving an opposite surface of the lead frame and the lead portions and the electrostatic discharge protection portion of the lead frame unencapsulated and further leaving a contact surface of the integrated circuit die exposed;

folding the electrostatic discharge protection portion of the lead frame around the encapsulated integrated circuit die.

Crane fails to teach folding the electrostatic discharge protection portion of the lead frame over or adjacent to a surface of the plastic or epoxy material as recited in present claim 21.

Ichikawa teaches the steps of folding a portion (Ichikawa outer portions Fig. 3 # 5 and # 6 of terminals # 2 and # 3 col. 1 line 56) of the lead frame (Ichikawa Fig. 3 # 11 col. 2 line 7) around sides of the encapsulated integrated circuit die (Ichikawa Fig. 1 # 4 Col. 1 line 52) and over or adjacent to a peripheral upper surface of the plastic or epoxy material (# 4), and Ichikawa further teaches the steps of folding portions (Ichikawa Fig. 4 # 32, # 33 col. 6 line 58) of the lead frame (Ichikawa Fig. 4 # 41 col. 6 line 47) around

each side (Fig. 4 col. 6 lines 52-61) of the encapsulated integrated circuit die (Ichikawa Fig. 4 # 31 col. 6 line 48). ***It would have been obvious to one of ordinary skill in the art of making semiconductor devices*** to incorporate Ichikawa teaching into Crane's method because in doing so a semiconductor device which is high in productivity and a lead frame which contributes to improvement in productivity of a semiconductor device can be obtained. See col. 3, lines 8-11.

4. Claims 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crane, Jr. et al. (U.S. Patent 6,307,258) in view of Ichikawa et al. (U.S. Patent 6,165,818).

Crane teaches a method of providing electrostatic discharge protection for an integrated circuit, comprising (See Col. 3, line 56 to col. 5, line 30 and FIGS. 1).

forming a flat lead frame 200 having lead portions 300 and an electrostatic discharge protection portion extending from edges thereof;

mounting the integrated circuit die 100 on the surface of the lead frame and encapsulating the at least sides of the integrated circuit die and a portion of the lead frame surface on which the integrated circuit die is mounted with an encapsulating material;

folding the electrostatic discharge protection portion of the lead frame around one or more sides of the encapsulating material and further comprising,

folding the electrostatic discharge protection portion of the lead frame to extend along the sides of the encapsulating material;

folding the electrostatic discharge protection portion of the lead frame to extend over a periphery of a surface or adjacent to a surface of the encapsulating material opposite the lead frame; and

folding the electrostatic discharge protection portion of the lead frame around at least two opposing sides of the encapsulating material.

Crane fails to teach leaving the lead portions and the electrostatic discharge protection portion of the lead frame projecting beyond and extending adjacent to a surface of the encapsulating opposite the lead frame the encapsulating material as recited in present claims 29 and 31.

Ichikawa teaches mounting an integrated circuit device 31 on a surface of the lead frame 41 having plurality of lead terminals 33 formed projecting beyond the encapsulating material 34 and the plurality of lead terminals are arranged at positions adjacent to the radiating terminals 32. See col. 6, lines 10-29 and FIGS. 4-7. ***It would have been obvious to one of ordinary skill in the art of making semiconductor devices*** to incorporate Ichikawa teaching into Crane's method because in doing so a semiconductor device which high in productivity and a lead frame which contributes to improvement in productivity of a semiconductor device can be obtained. See col. 3, lines 8-11.

Allowable Subject Matter

Claims 26-28 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies

(i.e., "A lead frame, as that term is employed in the specification and under the ordinary meaning of the term with the relevant art, is a structure, generally stamped from a metallic sheet, typically comprising a die paddle on which an integrated circuit die is mounted and lead portions extending outwardly thereform to project from the packaged integrated circuit after plastic or epoxy encapsulation of the integrated circuit die, die paddle, and part of each lead portion. The packaged integrated circuit leads are integrally formed from the lead frame) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaudhuri Olik can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
November 14, 2002